Performance degradation of GaN field-effect transistors due to thermal boundary resistance at GaN/substrate interface

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The authors investigate the effect of the thermal boundary resistance between the GaN layer and the substrate on the current–voltage characteristics of GaN MESFETs. Using material specific models for carrier drift-diffusion and thermal conductivity the authors determine the dependence of the breakdown voltage on thermal boundary resistance. The mechanism of the thermal breakdown in GaN transistors is also discussed. Obtained results can be used for structure optimisation of GaN-based transistors.

Introduction: GaN-based transistors attract significant attention from the device community due to their promise for microwave, high power, and other applications [1–3]. Heat removal is a major issue for all envisioned applications of GaN field-effect transistors. Despite the importance of thermal management for GaN technology, only limited experimental [4–5] and modelling work has been done [6]. In the continuous search for suitable substrates for GaN growth and recent experimental reports of unusually high thermal boundary resistance (TBR) between GaN and sapphire [7], an important question emerges: what is the effect of TBR between different layers of the GaN FET structure on the device current–voltage (I-V) characteristics. In this Letter we report results of our theoretical investigation that shed light on this issue.

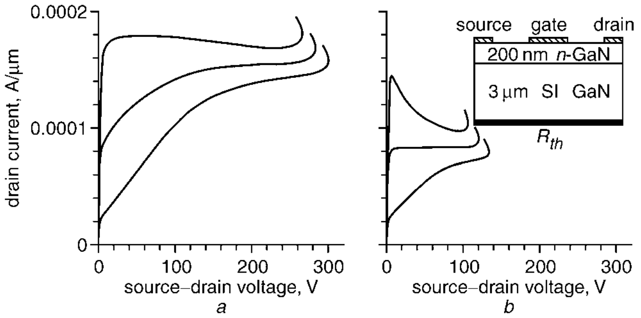

Fig. 1 *Drain current I_D against source–drain voltage V_{SD} for set of gate biases V_g from 0 (top curve) to -4 V (bottom curve) with 2 V step*

a $R_{th} = 0.001$ K cm^2/W *b* $R_{th} = 0.005$ K cm^2/W

Inset: schematic cross-section of GaN MESFET structure

Table 1: GaN materials and model parameters used in simulation

	Electrons	Holes
Relative permittivity: ε_r	9.5	
Lattice thermal conductivity: σ_T, W/(K cm)	1.55	
Lattice heat capacity: c_v, J/(K cm^3)	3.0	
Carrier effective mass: m^*/m_0	0.222	1.0
Bandgap energy: E_{G0}, eV	3.47	
α_G, eV/K	7.40×10^{-4}	
β_G, K	6.00×10^2	
α_0, cm^{-1}	2.9×10^8	1.34×10^8
b, V/cm	3.4×10^7	2.03×10^7
$\hbar\omega$, eV	0.035	
A, cm/s	2.10×10^7	
B, cm/s	2.94×10^6	
β_0	1.7	

Modelling approach: To investigate the effect of TBR on I–V characteristics of GaN transistors, we consider a typical n-type MESFET shown in the inset of Fig. 1. We choose the following parameters: the doping concentration in the active layer is 3×10^{17} cm^{-3}; thickness of the active layer is 200 nm; source–drain separation $L_{SD} = 5$ µm; gate length 1.6 µm. The active layer is on top of a 3 µm thick semi-insulating (SI) GaN buffer layer. Material and model parameters for GaN used in our simulation are summarised in Table 1. Two-dimensional simulations on the basis of the drift-diffusion model and thermal conduction equation have been performed using ISE TCAD DESSIS software with models and parameters specific for GaN. The MESFET structure can be modelled with the effective TBR lumped between the GaN epitaxial buffer layer and the substrate. The thermal conductivity of the GaN layer is known to depend strongly on the material quality, e.g. dislocation line density, impurity concentration [8]. The room temperature thermal conductivity K_{th} was assumed to be 1.55 W/cm K, which corresponds to crystalline GaN of typical quality. The $T^{-1/2}$ temperature dependence characteristic for GaN [8] has been taken into account. We used the standard model for the band gap energy temperature dependence $E_G = E_{G0} - \alpha T^2/(\beta + T)$. The ionisation coefficients were calculated using Van Overstraeten-de Man model

$$\alpha = \gamma\alpha_0 \exp\left\{\frac{-\gamma b}{E}\right\}, \quad \gamma = \frac{\tanh\{\hbar\omega/2kT_0\}}{\tanh\{\hbar\omega/2kT\}} \tag{1}$$

Here E is the electric field intensity, $\hbar\omega$ is the optical phonon energy, k is the Boltzmann constant, and $T_0 = 300$ K is the ambient temperature. For the mobility dependence on doping the μ_{low} model of [9] has been used under the assumption that the low field mobility in the undoped semiconductor is $\mu_{\max} = 1000$ cm^2/Vs. The high-field mobility has been calculated using the Canali model

$$\mu_{high} = \frac{\mu_{low}}{(1 + (\mu_{low}E/v_{sat})^{\beta_0})^{1/\beta_0}} \tag{2}$$

Here v_{sat} is the saturation velocity. The dependence of the saturation velocity on temperature, $v_{sat} = A – B(T/T_0)$, was obtained by fitting to the Monte Carlo simulation data [10].

We investigated I–V characteristics of GaN MESFET for a set of different TBR values. The choice of the TBR range is not straightforward. Experimental data for TBR at GaN/SiC and GaN/sapphire interfaces are scarce [6–7], and calculations can only be performed using acoustic-mismatch theory and the diffuse mismatch model (DMM). According to DMM calculations in [6], the TBR for GaN interface with relevant materials is about 10^{-5} W/cm K at room temperature. A recent experimental study [7] reported a TBR value of $R_{th} = 1.05$ K cm^2/W at 4.2 K, which, using the interpolation curve of [6] can be translated to approximately $R_{th} \sim 1 \times 10^{-3}$–$5 \times 10^{-3}$ K cm^2/W at room temperature. Thus, to elucidate the effect of TBR at the GaN layer–substrate interface, we examined the range of values from zero to 0.01 K cm^2/W.

Simulation results: Fig. 1 shows a set of I–V curves for the gate biases V_g from 0 to -4 V in 2 V steps for two cases: $R_{th} = 0.001$ K cm^2/W and $R_{th} = 0.005$ K cm^2/W. There is a pronounced negative slope region in the saturation current for zero gate biases in both cases. Its magnitude increases with increasing thermal boundary resistance. The latter is due to degradation of the carrier mobility as the temperature rises in the active layer. For example, at the onset of saturation region in the I–V curves shown in Fig. 1, the temperature is about $T = 400$ K for $R_{th} = 0.001$ K cm^2/W while it is about 500 K for $R_{th} = 0.005$ K cm^2/W ($V_g = 0$ V for both cases). One can also see in this Figure the degradation of the breakdown voltage V_B when TBR increases by a factor of five. To elucidate the breakdown mechanism in GaN-based transistors, we present in Fig. 2 the distributions of the electric field and hole concentration. The distributions are shown for bias conditions just before breakdown ($R_{th} = 0.001$ K cm^2/W, $V_g = 0$ V, $V_{SD} = 237$ V). The temperature of the hot spot under the drain is about 1000°C. One can clearly see two high field regions. The first is under the gate, from the drain side, and the second is under the drain. The maximum fields under the gate and drain are 5.1×10^6 V/cm, and 1.9×10^6 V/cm, respectively. This suggests that the thermal breakdown in GaN MESFETs is caused not only by the gate breakdown but also by the avalanche breakdown under the drain. Fig. 2*b* shows the beginning of the avalanche injection of holes into the SI GaN buffer. The negative differential resistance in the breakdown region of I–V curves is another indication of the avalanche injection-type breakdown of the drain. This breakdown mechanism is similar to the one observed in GaAs MESFETs [11].

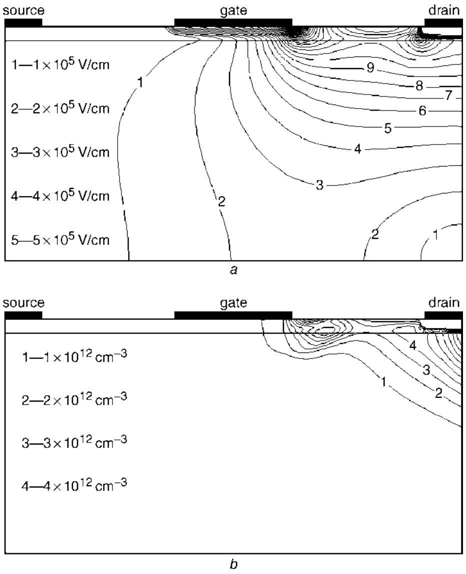

Fig. 2 *Distribution of electric field and hole concentration in GaN MESFET just before breakdown*

Thermal boundary resistance is assumed to be $R_{th} = 0.001$ K cm^2/W
a Electric field *b* Hole concentration

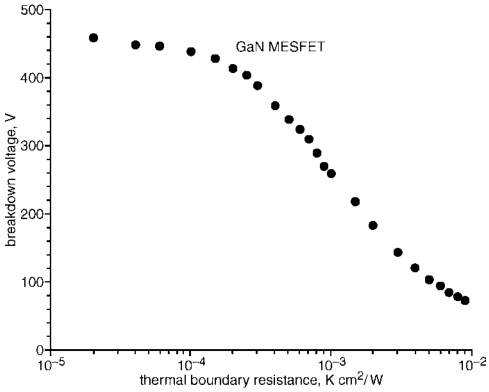

Fig. 3 *Breakdown voltage in GaN MESFET against thermal boundary resistance at GaN/substrate interface*

Table 2: Breakdown voltage in GaN MESFET

	$R_{th} = 0.001$ K cm^2/W	$R_{th} = 0.005$ K cm^2/W
V_{BR}, V ($V_g = 0$ V)	263	108
V_{BR}, V ($V_g = -2$ V)	281	120
V_{BR}, V ($V_g = -4$ V)	230	134

Fig. 3 presents the breakdown voltage dependence on TBR ($V_g = 0$ V). Note that for a device of given geometry and doping density in the ideal case of $R_{th} = 0$, the simulated breakdown voltage is as high as 470 V. The data on the V_B degradation for different gate bias values are summarised in Table 2. The increase of TBR from $R_{th} = 0.001$ K cm^2/W to $R_{\text{th}} = 0.005$ K cm^2/W results in a 40% decrease in the transconductance.

Conclusions: We have investigated the effect of thermal boundary resistance between the semi-insulating GaN layer and the substrate on *I–V* characteristics of GaN MESFET. It has been established that the breakdown voltage is very sensitive to the TBR value and at zero gate bias, decreases from 263 V to 108 V as TBR increases from $R_{th} = 0.001$ K cm^2/W to $R_{th} = 0.005$ K cm^2/W. This suggests that the performance of GaN power transistors can be significantly degraded due to relatively small variations in the quality of the interface between the GaN layer and the substrate. The nature of the thermal breakdown in GaN MESFETs has also been discussed.

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